CORRECTED AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listing of claims in the application:

Corrected Listing of Claims:

1. (Currently Amended) A chip scale package (CSP) structure for an image sensor, comprising:

a semi-conductor image sense chip;

multiple bonding pads formed on a top face of the semi-conductor image sense chip;

a conducting wire extending from each of the multiple bonding pads by wire-bonding; and

a liquefied gelatinous material covering the top face of the semi-conductor image sense chip and forming a transparent layer on the top face of the semi-conductor image sense chip after drying up, the transparent layer being a single layer structure coated over a top surface of said sense chip in a continuously contiguous manner, said transparent layer for permitting light to pass therethrough, having a thickness equal to a height of each of the conducting wire .

2. (Original) The CSP structure as claimed in claim 1, wherein the transparent layer comprises a top face ground and burnished to form a plane that is

parallel to the top face of the semi-conductor image sense chip and a periphery covered by a shelter to prevent the light from laterally penetrating into the chip scale package structure and influencing the quality of the images that is collected by the chip scale package structure.

3. (Previously Presented) The CSP structure as claimed in claim 2, wherein a metal solder ball is planted on a free end of each of the conducting wires and electrically connected to a flexible printed circuit (FPC), the FPC having a window defined therein and corresponding to a sensing area of the semi-conductor image sense chip and a conducting circuit formed on a bottom face of the FPC, the conducting circuit including multiple first solder points formed near a periphery of the window and the number of the first solder points corresponding to that of the conducting wire, the conducting circuit having multiple second solder points formed near one side of the FPC.

4. (Previously Presented) The CSP structure as claimed in claim 3, wherein the second solder points of the conducting circuit are arranged in an array.

5. (Currently Amended) A chip scale package (CSP) structure for an image sensor, comprising a semi-conductor image sense chip having multiple bumps formed on a top face of the semi-conductor image sense chip and a transparent layer ~~attached~~ continuously contiguous to the top face of the semi-conductor image sense chip, the transparent layer having a thickness being equal to that of each of the bumps for permitting light to pass therethrough.

6. (Previously Presented) The CSP structure as claimed in claim 5, wherein the transparent layer is a transparent glass plate including multiple penetration holes defined therein, each penetration hole aligning with a corresponding one of the multiple bumps such that each bump extends to a top face of the transparent glass plate.

7. (Previously Presented) The CSP structure as claimed in claim 6, wherein the transparent layer is a transparent glass plate having an area equal to that of the semi-conductor image sense chip, the transparent glass plate having a periphery covered by a shelter to prevent the light from laterally penetrating into the chip scale package structure and influencing the quality of the images collected by the chip scale package structure, wherein a metal solder ball is planted on a free end of each of the multiple bumps and electrically connected to a flexible printed circuit (FPC), the FPC having a window defined therein and corresponding to a sensing area of the semi-conductor image sense chip and a conducting circuit, the conducting circuit including multiple first solder points formed near a periphery of the window, the number of the first solder points corresponding to that of the bumps, the conducting circuit including multiple second solder points formed near one side of the FPC.

8. (Previously Presented) The CSP structure as claimed in claim 5, wherein said transparent layer is made from a gelatinous liquefied material covering the top face of the semi-conductor image sense chip and dried up.

9. (Original) The CSP structure as claimed in claim 8, wherein the transparent layer comprises a top face ground and burnished to form a plane that is parallel to the top face of the semi-conductor image sense chip and a periphery covered by a shelter to prevent the light from laterally penetrating into the chip scale package structure and influencing the quality of the images that is collected by the chip scale package structure.

10. (Previously Presented) The CSP structure as claimed in claim 9, wherein a metal solder ball is planted on a free end of each of the multiple bumps and is electrically connected to a flexible printed circuit (FPC), the FPC having a window defined therein and corresponding to a sensing area of the semi-conductor image sense chip and a conducting circuit, the conducting circuit including multiple first solder points formed near a periphery of the window, the number of the first solder points corresponding to that of the multiple bumps, the conducting circuit including multiple second solder points formed near a side of the FPC.